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| **Title: ACCEPTANCE TEST PROCEDURE for PCB, Gantry POWER Distribution ASSEMBLY**    **P/N’s P1060960-xxx** | | |
| **Customer: Varian Medical Systems** | | |

*Content: This document describes the procedure for functional testing of the PCB, Gantry POWER Distribution ASSY.P/N P1060960-xxx*

**REVISION HISTORY**

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# PURPOSE

This document provides step-by-step functional testing methods for automatic testing of the PCB, Gantry POWER Distribution Assembly on the SOCRATES ATE System of Jabil Circuit Inc, which is located at the Tempe, Arizona plant. The following tests and inspections are performed:

## SOCRATES Functional Test

* Monitor Signals Pass thru Test
* Power - up Test
* AC Loads Test
* Collimator Test
* DC Loads Test
* DC Spares AC Service Test
* Gantry Cabinet Test
* Imaging DC Power Test
* Lamps Test

# SCOPE

This document constitutes the SOCRATES functional test plan for the PCB, Gantry POWER Distribution Assy., P/N P1060960-xxx. This document describes the testing procedures in a high level format without making detailed references to the test software, instrument configuration or ATE stimulus and response signal routing. Units that meet all of the requirements of this document shall be accepted as functional.

# REFERENCE DOCUMENTS

* Schematic – PCB, Gantry POWER Distribution SCHEMATIC, P/N P1060961.
* BOM and Fab Drawing – PCB Gantry POWRE Distribution Assy., P1060963 and P1060965.
* Test Fixture Schematic – PCB, Gantry POWER Distribution Assy., P/N P1060960-FX.
* Schematic – DTR Power Distribution, P/N 100025093.
* SOCRATES Automated Functional Test System Documentation.

# DEFINITIONS

|  |  |
| --- | --- |
| ATE | Automatic Test Equipment |
| ESD | Electro-Static Discharge |
| GND | Ground/UUT 0V Reference |
| P/N | Part Number |
| PCB | Printed Circuit Board |

UUT Unit Under Test

Vdc Volts Direct Current

Vac Volts Alternating Current

LSB Least Significant Bit

MSB Most Significant Bit

DPD\_PCB DTR POWER DISTRIBUTION board

# EQUIPMENT REQUIRED

The following list contains the required test equipment for functional testing of the PCB Gantry POWER Distribution Assy., P/N P1060960-xxx on the SOCRATES ATE System.

## SOCRATES Test Equipment

5.1.1 VMS DTR POWER DISTRIBUTION Assembly gold board (P/N: 100025092)

5.1.2 N6742A - Agilent DC Power Module 8V / 12.5A

5.1.3 N6744A - Agilent DC Power Module 35V/ 3.0A

5.1.4 6744A - Agilent DC Power Supply 60V / 35A

5.1.5 6744A - Agilent DC Power Supply 60V / 35A

5.1.6 1251RP California Instrument 1250VA AC Power Supply

5.1.7 34410A - Agilent Digital Multimeter

5.1.8 DSO6014L – 4 channel 100MHz Oscilloscope

5.1.9 PXI6509 – National Instrument 96 channel DIO

5.1.10 PXI2527 – National Instrument 32 channel MUX module

5.1.11 PXI2566 – National Instrument 16 channel high current relay

5.1.12 PXI2568 – National Instrument 32 channel high current relay

5.1.13 PLZ1004W – Kikusui 1000W Electronic load

## Test Software/Firmware

5.2.1 Test Program Software, P/N 100020922-TSW – developed with Microsoft Visual Studio.Net 2010

5.2.2 ~~Test Fixture Firmware, P/N MCF5282-TFW – developed with GNU C/C++ cross complier tool chain for ColdFire~~

5.2.3 Test Firmware, P/N 100025092-TFW – developed with Texas Instruments Code Composer Studio

3.1 tool chain for C2000 DSP

# PRE-TEST PROCEDURES

***Warning: ESD Sensitive devices present* -** Ensure proper grounding procedures are followed while handling/testing this and all ESD sensitive assemblies as defined in IPC-A-610.

## Visual Inspection

6.1.1 Visually inspect the PCB, Gantry POWER Distribution Assy. to be tested for obvious signs of wrong, missing or improperly oriented parts (Refer to Assembly Drawing)

6.1.2 Also inspect for signs of contamination and poor workmanship including soldering defects (bridges,

splashes, balls, unsoldered pins, flux build-up, etc.) and improper mounting of parts. Pay specific attention to ensure that through-hole parts and sockets are mounted flush to the board

6.1.3 Any discrepancies must be corrected before proceeding

# TEST SETUP

## ATE/Fixture Connections and Software Loading - Performed once for each lot.

7.1.1 Ensure that all instruments on the SOCRATES ATE Test Rack have been reset

7.1.2 Ensure that the engaging handle on the ATE Interface is in the up (disengaged) position

7.1.3 Place the PCB, Gantry POWER Distribution Board Test Fixture, P/N P1060960-FX, on to the interface with the fixture hinges facing the machine. Connect the RS232 cable to the D-sub located at left side of the test fixture

7.1.4 Once the fixture is properly seated on the interface, push the interface handle down to engage the fixture

7.1.5 On the SOCRATES ATE Test Rack Computer, load PCB, Gantry POWER Distribution Board test program P1060960-TSW (if not already loaded) by clicking on the START button on the taskbar. Select the Production folder to display the entire sub-folder. In the VMS sub-folder, Double click on the P1060960-TSW to launch the test software

## UUT/Fixture Connections - Performed for each board.

7.2.1 Place the UUT onto the test fixture such that the fixture standoffs match up with the UUT mounting holes.

7.2.2 Connect the fixture cable headers J1, J2, J4, J5, J7, J14 through J17, J20 through J23, J38, J39, J42, J44 through J47, J49 and J50 to UUT headers J1, J2, J4, J5, J7, J14 through J17, J20 through J23, J38, J39, J42, J44 through J47, J49 and J50 respectively.

7.2.3 Place the DTR POWER DISTRIBUTION (VMS: 100025092) board onto the headers J6, J8 and J35 of the UUT

7.2.4 When all the necessary connections have been made, click on the START button on the test program GUI to start the test

# TEST PROCEDURE

The following procedure contains step-by-step instructions for testing the UUT. Although this test was developed exclusively to be performed on a specific ATE (SOCRATES ATE System), it does not detail the specific ATE related operations such as signal routing. This information could be gathered by inspection of the test software and fixture drawing.

Note: The test is performed with the utilization of the test firmware that resides at the DSP of the DTR POWER DISTRIBUTION board (DPD\_PCB). The two applications communicate with each other over the CAN bus established between the DPD\_PCB and the interface board residing inside the test fixture.

## Pass – Thru Test

This test will verify pass - thru connections from the connectors J15, J21, J22, J20 and J14 to the connectors J16 and J23 of the UUT. During the test bit patterns will be written to the connectors J15, J21, J22, J20, and J14, and then the bit patterns will be read from the connectors J16 and J23. The pass – thru connections will be verified for shorts and opens using bit patterns. Table 1 shows the bit assignment for the connectors. Refer to sheet 7 of the UUT schematic.

|  |  |  |  |
| --- | --- | --- | --- |
| Bit | Input Terminals | Output Terminals | Output Terminals |
| 0 | J15-1 | J16-1 |  |
| 1 | J15-9 | J16-2 |  |
| 2 | J15-2 | J16-3 |  |
| 3 | J15-10 | J16-4 |  |
| 4 | J15-3 | J16-5 |  |
| 5 | J15-11 | J16-6 |  |
| 6 | J15-4 | J16-7 |  |
| 7 | J15-12 | J16-8 |  |
| 8 | J15-5 | J16-11 | J23-1 |
| 9 | J15-13 | J16-12 | J23-2 |
| 10 | J15-6 | J16-9 |  |
| 11 | J15-14 | J16-10 |  |
| 12 | J21-1 | J16-15 |  |
| 13 | J21-2 | J16-16 |  |
| 14 | J22-1 | J16-17 |  |
| 15 | J22-2 | J16-18 |  |
| 16 | J20-1 | J16-13 |  |
| 17 | J20-2 | J16-25 |  |
| 18 | J14-1 | J16-23 |  |
| 19 | J14-6 | J16-24 |  |
| 20 | J14-2 | J16-21 |  |
| 21 | J14-7 | J16-22 |  |

**Table 1 Pass – Thru Table**

8.1.1 A bit pattern 0x155555 will be written to J15, J21, J22, J20, and J14 (input connectors). The bit pattern will be verified from J16 for 0x0x155555 (output connector)

8.1.2 The bit patter will be verified from J23 for 0x1 (output connector)

8.1.3 A bit pattern 0x2AAAAA will be written to J15, J21, J22, J20, and J14 (input connectors). The bit pattern will be verified from J16 for 0x0x2AAAAA (output connector)

8.1.4 The bit patter will be verified from J23 for 0x2 (output connector)

8.1.5 A bit pattern 0x3BBBBB will be written to J15, J21, J22, J20, and J14 (input connectors). The bit pattern will be verified from J16 for 0x3BBBBB (output connector)

8.1.6 The bit patter will be verified from J23 for 0x3 (output connector)

## Power - Up Test

This test will verify that the UUT powers up and the DSP boots up successfully. The +28Vdc and +24Vdc will be measured and verified to be within tolerance. The status of the 28Vdc and the 24Vdc are monitored by D15, D25 and D28. Refer to sheet 2, sheet 7, and sheet 8 of the UUT schematic.

8.2.1 +24.0Vdc will be applied between J1-1, 2 (+24VIN) and J1-4 (24VRTN) with DC #5

8.2.2 +28.0Vdc will be applied between J2-1, 2 (+28VF) and J2-3 (28VRTN) with DC #9

8.2.3 The voltage at J1-1 (+24VIN) will be measured for 24Vdc ± 1Vdc

8.2.4 The voltage at J2-1 (+28VF) will be measured for 28Vdc ± 1Vdc

8.2.5 The voltage at J35-34 (24VMTR) will be measured from the signal terminal AI\_MF1 on the DPD\_PCB for 0.889Vdc ± 0.05Vdc

8.2.6 The voltage at J35-36 (28VMTR) will be measured from the signal terminal AI\_MF3 on the DPD\_PCB for 0.711Vdc ± 0.035Vdc

8.2.7 A logic high will be applied to J17-9 (SYNC\_A), and a logic low will be applied to J17-10 (SYNC\_B)

8.2.8 The signal at SYNC\_I on the DPD\_PCB will be measured for logic high

8.2.9 A logic low will be applied to J17-9 (SYNC\_A), and a logic high will be applied to J17-10 (SYNC\_B)

8.2.10 The signal at SYNC\_I on the DPD\_PCB will be measured for logic low

8.2.11 Close relay channel 24, +24V will be applied between J17-5 and 24VRTN

8.2.12 The voltage at J35-37 (MEL\_IN) will be measured for 4.0±0.5Vdc

8.2.13 Open relay channel 24, +24V will be removed between J17-5 and 24VRTN

8.2.14 Verify that D15, D25, and D28 are illuminated

## AC Loads Test

This test will verify the operation of the AC loads circuit, which mainly consists of RL1~RL9, AC\_MON3~AC\_MON6, AC\_MON9, AC\_MON10, D55~D58, D71, D72, D74, D75, D77, D78, D80, D81 and D84. During the test, RL1~RL9 will be turned on; and the status of the 120Vac will be monitored through optical isolator AC\_MON3~AC\_MON6, AC\_MON9, AC\_MON10 by D55~D58, D71, D81. The relevant the signals will be measured and verified to be within tolerance. Refer to the sheet 3 and sheet 10 of the UUT schematic.

8.3.1 120Vac will be applied between J1-13 (CONTPWRA) and J1 14 (ACCOM) with AC #1

8.3.2 120Vac will be applied between J1-15 (CONTPWRB) and J1-14 (ACCOM) with AC #2

8.3.3 The signal at J8-21 (CONTPWRASTS) will be measured for logic high

8.3.4 The signal at J8-22 (CONTPWRBSTS) will be measured for logic high

8.3.5 The voltage at J47-1 (IONGAUGEPWR) will be measured for 120Vac ± 10Vac

8.3.6 The voltage at J44-4 (GUNDPWR1) will be measured for 120Vac ± 10Vac

8.3.7 The voltage at J44-6 (GUNDPWR2) will be measured for 120Vac ± 10Vac

8.3.8 Verify that D46, D45, D72, D74 and D84 are illuminated

8.3.9 0Vdc will be applied to J6-12 (SPAREAC2ON), J6-34 (FANAC2ON), and J35-13 (PWRSHLF2ON)

8.3.10 +22.6Vdc will be applied to J6-9 (SPAREAC1ON), J6-33 (FANAC1ON), J35-14 (PWRSHLF1ON) and J6-39 (DUON)

8.3.11 The voltage at J44-7 (ACSPARE1) will be measured for 120Vac ± 10Vac

8.3.12 The voltage at J44-10 (ACSPARE2) will be measured for 0Vac ± 1Vac

8.3.13 The voltage at J44-12 (ACFAN1) will be measured for 120Vac ± 10Vac

8.3.14 The voltage at J44-14 (ACFAN2) will be measured for 0Vac ± 1Vac

8.3.15 With a 150Ω fixture mounted load connected to ACFAN1 J44-12, set AC input CONTPWRA to 60VAC; Measure output AI\_MF7, J35-40 for 0.670VDC +/-10%; Note: This measurement is made through a divide by 2 circuit on the 100025092 Daughter Card, actual voltage on the UUT is twice the measured value.

8.3.16 With a 150Ω fixture mounted load connected to ACFAN1 J44-12, set AC input CONTPWRA to 90VAC; Measure output AI\_MF7, J35-40 for 0.960VDC +/-10%; Note: This measurement is made through a divide by 2 circuit on the 100025092 Daughter Card, actual voltage on the UUT is twice the measured value.

8.3.17 With a 150Ω fixture mounted load connected to ACFAN1 J44-12, set AC input CONTPWRA to 120VAC; Measure output AI\_MF7, J35-40 for 1.210VDC +/-10%; Note: This measurement is made through a divide by 2 circuit on the 100025092 Daughter Card, actual voltage on the UUT is twice the measured value.

8.3.18 The voltage at J38-1 (PWRSHELF1) will be measured for 120Vac ± 10Vac

8.3.19 The voltage at J38-7 (PWRSHELF2) will be measured for 0Vac ± 1Vac

8.3.20 The voltage at J38-9 (DU) will be measured for 120Vac ± 10Vac

8.3.21 The voltage at J38-11 (OILPMP) will be measured for 120Vac ± 10Vac

8.3.22 The signal at J8-10 (PWRSHLF1STS) will be measured for logic high

8.3.23 The signal at J8-11 (PWRSHLF2STS) will be measured for logic low

8.3.24 The signal at J8-12 (DUSTS) will be measured for logic high

8.3.25 The signal at J8-13 (OILPMPSTS) will be measured for logic high

8.3.26 Verify that D55, D56, D58, D75, and D80 are illuminated, and D57, D77, and D78 are not illuminated

8.3.27 +22.6Vdc will be applied to J6-12 (SPAREAC2ON), J6-34 (FANAC2ON), and J35-13 (PWRSHLF2ON)

8.3.28 0Vdc will be applied to J6-9 (SPAREAC1ON), J6-33 (FANAC1ON), J35-14 (PWRSHLF1ON), and J6-39 (DUON)

8.3.29 The voltage at J44-7 (ACSPARE1) will be measured for 0Vac ± 1Vac

8.3.30 The voltage at J44-10 (ACSPARE2) will be measured for 120Vac ± 10Vac

8.3.31 The voltage at J44-12 (ACFAN1) will be measured for 0Vac ± 1Vac

8.3.32 The voltage at J44-14 (ACFAN2) will be measured for 120Vac ± 10Vac

8.3.33 The voltage at J38-1 (PWRSHELF1) will be measured for 0Vac ± 1Vac

8.3.34 The voltage at J38-7 (PWRSHELF2) will be measured for 120Vac ± 10Vac

8.3.35 The voltage at J38-9 (DU) will be measured for 0Vac ± 1Vac

8.3.36 The voltage at J38-11 (OILPMP) will be measured for 120Vac ± 10Vac

8.3.37 The signal at J8-10 (PWRSHLF1STS) will be measured for logic low

8.3.38 The signal at J8-11 (PWRSHLF2STS) will be measured for logic high

8.3.39 The signal at J8-12 (DUSTS) will be measured for logic low

8.3.40 The signal at J8-13 (OILPMPSTS) will be measured for logic high

8.3.41 Verify that D57, D77, and D78 are illuminated, D55, D56, D58, D75, and D80 are not illuminated

8.3.42 0Vdc will be applied to J6-20 (GNT\_MONPWRON) and J6-21 (MLCPWRON)

8.3.43 The voltage at J5-8 (GNT\_MONPWR) and J5-7 (MLCPWR) will be measured for 0Vac ± 1Vac

8.3.44 The signal at J8-9 (GNT\_MONPWRSTS) and J8-8 (MLCPWRSTS) will be measured for logic low

8.3.45 Verify that D71 and D81 is not illuminated

8.3.46 +22.6Vdc will be applied to J6-20 (GNT\_MONPWRON) and J6-21 (MLCPWRON)

8.3.47 The voltage at J5-8 (GNT\_MONPWR) and J5-7 (MLCPWR) will be measured for 120Vac ± 10Vac

8.3.48 The signal at J8-9 (GNT\_MONPWRSTS) and J8-8 (MLCPWRSTS) will be measured for logic high

8.3.49 Verify that D71 and D81 is illuminated Green Light

8.3.50 The 120Vac will be removed between J1-13 (CONTPWRA) and J1-14 (ACCOM)

8.3.51 The 120Vac will be removed between J1-15 (CONTPWRB) and J1-14 (ACCOM)

8.3.52 The voltage at J47-1 (IONGAUGEPWR) will be measured for 0Vac ± 1Vac

8.3.53 The voltage at J44-4 (GUNDPWR1) will be measured for 0Vac ± 1Vac

8.3.54 The voltage at J44-6 (GUNDPWR2) will be measured for 0Vac ± 1Vac

8.3.55 The voltage at J38-11 (OILPMP) will be measured for 0Vac ± 1Vac

## Collimator Test

This test will verify the operation of the collimator circuit, which consists of U31. During the test, the switch U31 will be turned on. The relevant signals will be measured and verified to be within tolerance. Resistive load will be applied to the outputs at J4. Refer to the sheet 4 of the UUT schematic.

8.4.1 +22.6Vdc is applied to J6-22 (COLLCTRLON#)

8.4.2 Close relay SW1 to apply electronic load to J4-1(COLL)

8.4.3 0Vdc will be applied to J6-22 (COLLCTRLON#)

8.4.4 The voltage at J4-1, J4-3 and J4-4 (COLL) will be measured for 24Vdc ± 0.5Vdc

8.4.5 Verify D52 is illuminated

8.4.6 Turn on electronic load and set current to 2.4Amps

8.4.7 The voltage at J4-1 (COLL) will be measured for 24Vdc ± 0.5Vdc with load

8.4.8 Turn off the electronic load

8.4.9 Open SW1 to disconnect the load.

8.4.10 +22.6Vdc will be applied to J6-22 (COLLCTRLON#)

8.4.11 The voltage at J4-1 (COLL) will be measured for 0Vdc ± 0.5Vdc

8.4.12 Verify D52 is not illuminated

## DC Loads Test

This test will verify the operation of the DC loads circuit, which consists of U60, U33 and U32. During the test, the switches U33 and U32 will be turned on; and the switch U60 will be turned on by the high signal FAN28V2ON. The relevant signals will be measured and verified to be within tolerance, and D67, D53 and D54 will be visually verified. Resistive load will be applied to the BGM\_EGN and VACION PS outputs at J39. Refer to sheet 5 of the UUT schematic.

8.5.1 Make sure +22.6Vdc is applied to J6-8 (VACON#) and J6-7 (BGMEGNON#), 0Vdc is applied to J1-3 (EMO\_GOOD)

8.5.2 Set 28DCPS\_ENAB and 4896DCPS\_ENAB high

8.5.3 J6-25 (FAN28V2ON) is default low.

8.5.4 J50-6 (4896DCPS\_ENAB) will be measured for 3.3Vdc ± 0.5Vdc and D13 is illuminated

8.5.5 J50-5 (DCPS28\_ENAB) will be measured for 3.3Vdc ± 0.5Vdc and D14 is illuminated

8.5.6 The voltage at J39-3 (FAN28V1) and J39-8 (FAN28V2) will be measured for 0Vdc ± 0.5Vdc

8.5.7 Verify that D67 is not illuminated

8.5.8 Set 28DCPS\_ENAB and 4896DCPS\_ENAB low

8.5.9 Close tester relay SW to apply electronic load to J39-3 (FAN28V1)

8.5.10 +22.6Vdc will be applied to J6-25 (FAN28V2ON)

8.5.11 The voltage at J39-3 (FAN28V1) and J39-8 (FAN28V2) will be measured for 27Vdc to 30.0Vdc without load

8.5.12 Turn on electronic load and set current to 1.0Amps

8.5.13 The voltage at J39-3 (FAN28V1) and J39-8 (FAN28V2) will be measured for 27Vdc to 30.0Vdc with load

8.5.14 Turn off the electronic load

8.5.15 J50-6 (4896DCPS\_ENAB) will be measured for 0Vdc ± 0.5Vdc and D13 is not illuminated

8.5.16 J50-5 (DCPS28\_ENAB) will be measured for 0Vdc ± 0.5Vdc and D14 is not illuminated

8.5.17 Verify that D67 is illuminated green light

8.5.18 Open tester relay SW to disconnect the load.

8.5.19 J39-5 (FAN1STS) will be connected to 28VRTN

8.5.20 The signal at J8-24 (FAN28V1FANULT) will be measured for logic high

8.5.21 The signal at J8-25 (FAN28V2FANULT) will be measured for logic low

8.5.22 J39-5 (FAN1STS) will be disconnected from 28VRTN

8.5.23 J39-10 (FAN2STS) will be connected to 28VRTN

8.5.24 The signal at J8-24 (FAN28V1FANULT) will be measured for logic low

8.5.25 The signal at J8-25 (FAN28V2FANULT) will be measured for logic high

8.5.26 J39-10 (FAN2STS) will be disconnected from 28VRTN

8.5.27 Close relay SW4 to apply electronic load to J39-12(BGM\_EGN)

8.5.28 +22.6Vdc will be removed from J6-7 (BGMEGNON#)

8.5.29 The voltage at J39-12 (BGMEGN) will be measured for 24Vdc ± 1Vdc without load

8.5.30 The voltage at J39-14 (VAC) will be measured for 0Vdc ± 0.5Vdc

8.5.31 Verify that D54 is illuminated green and D53 is not illuminated

8.5.32 Turn on electronic load and set current to 2.4Amps

8.5.33 The voltage at J39-12 (BGMEGN) will be measured for 24Vdc ± 1Vdc with load

8.5.34 Turn off the electronic load

8.5.35 The signal at J8-20 (VACSTS) will be measured for logic low

8.5.36 +22.6Vdc will be applied from J6-7 (BGMEGNON#)

8.5.37 Open SW4 to disconnect the load.

8.5.38 Close relay SW5 to apply electronic load to J39-14 (VAC)

8.5.39 +22.6Vdc will be removed from J6-8 (VACON#)

8.5.40 The voltage at J39-14 (VAC) will be measured for 0Vdc ± 0.5Vdc

8.5.41 +24.0Vdc will be applied to J1-3 (EMO\_GOOD)

8.5.42 The voltage at J39-12 (BGMEGN) will be measured for 0Vdc ± 0.5Vdc

8.5.43 The voltage at J39-14 (VAC) will be measured for 24Vdc ± 1Vdc with no load

8.5.44 Verify that D54 is not illuminated and D53 is illuminated green

8.5.45 Turn on electronic load and set current to 2.4Amps

8.5.46 The voltage at J39-14 (VAC) will be measured for 24Vdc ± 1Vdc with load

8.5.47 Turn off the electronic load

8.5.48 The signal at J8-20 (VACSTS) will be measured for logic high

8.5.49 The +24.0Vdc will be removed from J1-3 (EMO\_GOOD)

8.5.50 +22.6Vdc will be applied from J6-8 (VACON#)

8.5.51 Open SW5 to disconnect the load.

## DC Spares and AC Service Test

This test will verify the operation of the DC Spare AC service circuit, which consists of U43, U44, U27, U28, U25, U26 and D69. During the test, the switches U43, U44, U27, U28 will be turned on. The relevant signals will be measured and verified within tolerance, and D12, D33, D34 and D35 and D69 will be visually verified. Resistive load will be applied to the Spare Power outputs at J45. Refer to the sheet 6 and sheet 4 of the UUT schematic.

8.6.1 Make sure that 0Vdc is applied to J35-9 (COLLAMP2ON), J35-10 (COLLAMP1ON), J35-11 (SPARE28V2ON), and J35-12 (SPARE28V1ON)

8.6.2 120Vac will be applied between J1-13 (CONTPWRA) and J1-14 (ACCOM) with AC #1

8.6.3 The voltage at J7-1 (ACSEVICE) will be measured for 120Vac ± 10Vac

8.6.4 Verify that D69 is illuminated green light

8.6.5 The 120Vac will be removed between J1-13 (CONTPWRA) and J1-14 (ACCOM)

8.6.6 A logic high signal will be applied to J45-9 (SPAREIN1\_), and a logic low will be applied to J45-11 (SPAREIN2\_)

8.6.7 The signal at J8-17 (SPAREIN1) will be measured for logic high

8.6.8 The signal at J8-18 (SPAREIN2) will be measured for logic low

8.6.9 A logic low signal will be applied to J45-9 (SPAREIN1\_), and a logic high will be applied to J45-11 (SPAREIN2\_)

8.6.10 The signal at J8-17 (SPAREIN1) will be measured for logic low

8.6.11 The signal at J8-18 (SPAREIN2) will be measured for logic high

8.6.12 Close relay SW15 to apply 9.3 ohm resistive load to J45-1 (SPARE28V1)

8.6.13 +22.6Vdc will be applied to J35-12 (SPARE28V1ON)

8.6.14 Turn on the electronic load

8.6.15 The voltage at J45-1 (SPARE28V1) will be measured for 27Vdc to 30.0Vdc

8.6.16 The voltage at J45-3 (SPARE28V2) will be measured for 0Vdc ± 0.5Vdc

8.6.17 Verify that D35 is illuminated green and D12 is not illuminated

8.6.18 Turn off the electronic load

8.6.19 The signal at J8-15 (SPARE28V1STS) will be measured for logic high

8.6.20 The signal at J8-16 (SPARE28V2STS) will be measured for logic low

8.6.21 +22.6Vdc will be removed from J35-12 (SPARE28V1ON)

8.6.22 Open SW15 to disconnect the load.

8.6.23 Close relay SW16 to apply resistive load to J45-3 (SPARE28V2)

8.6.24 +22.6Vdc will be applied to J35-11 (SPARE28V2ON)

8.6.25 Turn on the electronic load

8.6.26 The voltage at J45-1 (SPARE28V1) will be measured for 0Vdc ± 0.5Vdc

8.6.27 The voltage at J45-3 (SPARE28V2) will be measured for 27Vdc to 30.0Vdc

8.6.28 Verify that D35 is not illuminated and D12 is illuminated green

8.6.29 Turn off the electronic load

8.6.30 The signal at J8-15 (SPARE28V1STS) will be measured for logic low

8.6.31 The signal at J8-16 (SPARE28V2STS) will be measured for logic high

8.6.32 +22.6Vdc will be removed from J35-11 (SPARE28V2ON)

8.6.33 Open SW16 to disconnect the load.

8.6.34 Close relay SW17 to apply resistive load to J45-5 (COLL1LAMP24V)

8.6.35 +22.6Vdc will be applied to J35-10 (COLLAMP1ON)

8.6.36 Turn on the electronic load

8.6.37 The voltage at J45-5 (COLL1LAMP24V) will be measured for 24Vdc ± 0.5Vdc

8.6.38 The voltage at J45-7 (COLL2LAMP24V) will be measured for 0Vdc ± 0.5Vdc

8.6.39 Verify that D34 is illuminated green and D33 is not illuminated

8.6.40 Turn off the electronic load

8.6.41 +22.6Vdc will be removed from to J35-10 (COLLAMP1ON)

8.6.42 Open SW17 to disconnect the load.

8.6.43 Close relay SW18 to apply resistive load to J45-7 (COLL2LAMP24V)

8.6.44 +22.6Vdc will be applied to J35-10 (COLLAMP1ON)

8.6.45 Turn on the electronic load

8.6.46 The voltage at J45-5 (COLL1LAMP24V) will be measured for 0Vdc ± 0.5Vdc

8.6.47 The voltage at J45-7 (COLL2LAMP24V) will be measured for 24Vdc ± 0.5Vdc

8.6.48 Verify that D34 is not illuminated and D33 is illuminated green

8.6.49 Turn off the electronic load

8.6.50 +22.6Vdc will be removed from to J35-10 (COLLAMP1ON)

8.6.51 Open SW18 to disconnect the load.

## Gantry Cabinet Test

This test will verify the operation of the gantry cabinet circuit, which consists of U18, U21, U36~U39, U20 and U34. During the test, the switches U21, U36~U39 will be turned on, and the FETs U20 and U34 will be turned off. The relevant signals will be measured and verified to be within tolerance, and D17 through D21 will be visually verified. Resistive load will be applied to the Gantry Cabinet Power outputs at J46. Refer to the sheet 8 of the UUT schematic.

8.7.1 Make sure +22.6Vdc is applied to J6-10 (BGMCONTON#), J6-11 (BGMPWMON#), and J6-13 (BGMPOSON#)

8.7.2 Program the electronic load to draw 2.4 Amp current

8.7.3 Close relay SW10 to apply electronic load to J46-1 (BGMCONT)

8.7.4 +22.6Vdc will be removed from J6-10 (BGMCONTON#),

8.7.5 Turn on the electronic load

8.7.6 The voltage at J46-1 (BGMCONT) will be measured for 24Vdc ± 1Vdc

8.7.7 The voltage at J46-3 (BGMPWM) will be measured for 0Vdc ± 0.5Vdc

8.7.8 The voltage at J46-5 (BGMPWMPWR) will be measured for 0Vdc ± 0.5Vdc

8.7.9 Verify that D20 is illuminated Green Light, and D21 is not illuminated

8.7.10 Turn off the electronic load

8.7.11 +22.6Vdc will be applied to J6-10 (BGMCONTON#),

8.7.12 Open SW10 to disconnect the load.

8.7.13 Close relay SW11 to apply electronic load to J46-3 (BGMPWM)

8.7.14 +22.6Vdc will be removed from J6-11 (BGMPWMON#)

8.7.15 Turn on the electronic load

8.7.16 The voltage at J46-1 (BGMCONT) will be measured for 0Vdc ± 0.5Vdc

8.7.17 The voltage at J46-3 (BGMPWM) will be measured for 24Vdc ± 1Vdc

8.7.18 Verify that D20 is not illuminated, and D21 is illuminated Green Light

8.7.19 Turn off the electronic load

8.7.20 Open SW11 to disconnect the load.

8.7.21 Program the electronic load to draw 5.6A current

8.7.22 Close relay SW7 to apply electronic load to J46-5 (BGMPWMPWR)

8.7.23 Turn on the electronic load

8.7.24 The voltage at J46-5 (BGMPWMPWR) will be measured for 27Vdc to 30Vdc

8.7.25 The voltage at J46-7 (BGMPOS) will be measured for 0Vdc ± 0.5Vdc

8.7.26 The voltage at J46-9 (BGMPOSPWR) will be measured for 0Vdc ± 0.5Vdc

8.7.27 Verify that D18 is not illuminated

8.7.28 Turn off the electronic load

8.7.29 The signal at J8-3 (BGMPWMPWRSTS) will be measured for logic high

8.7.30 The signal at J8-2 (BGMPOSPWRSTS) will be measured for logic low

8.7.31 Verify that D19 is illuminated Green Light, and D17 is not illuminated

8.7.32 +22.6Vdc will be applied to J6-11 (BGMPWMON#)

8.7.33 Open SW7 to disconnect the load.

8.7.34 Program the electronic load to draw 2.4 Amp current

8.7.35 Close relay SW12 to apply electronic load to J46-7 (BGMPOS)

8.7.36 +22.6Vdc will be removed from J6-13 (BGMPOSON#)

8.7.37 Turn on the electronic load

8.7.38 The voltage at J46-7 (BGMPOS) will be measured for 24Vdc ± 1Vdc

8.7.39 Verify that D18 is illuminated Green Light

8.7.40 Turn off the electronic load

8.7.41 Open SW12 to disconnect the load.

8.7.42 Program the electronic load to draw 5.6A current

8.7.43 Close relay SW8 to apply electronic load to J46-9 (BGMPOSPWR)

8.7.44 Turn on the electronic load

8.7.45 The voltage at J46-9 (BGMPOSPWR) will be measured for 27Vdc to 30Vdc

8.7.46 Turn off the electronic load

8.7.47 The signal at J8-3 (BGMPWMPWRSTS) will be measured for logic low

8.7.48 The signal at J8-2 (BGMPOSPWRSTS) will be measured for logic high

8.7.49 Verify that D17 is illuminated Green Light, and D19 is not illuminated

8.7.50 +22.6Vdc will be applied to J6-13 (BGMPOSON#)

8.7.51 Open SW8 to disconnect the load.

8.7.52 Program the electronic load to draw 2.4A current

8.7.53 Close tester relay SW to apply electronic load to J46-12 (FAN24V1)

8.7.54 Turn on the electronic load

8.7.55 The voltage at J46-12 (FAN24V1) will be measured for 24Vdc ± 0.5Vdc

8.7.56 The voltage at J46-14 (FAN24V2) will be measured for 24Vdc ± 0.5Vdc

8.7.57 Turn off the electronic load

8.7.58 Open tester relay SW to disconnect the load.

## Imaging DC Test

This test will verify the operation of the imaging DC circuit, which consists of U11~U15 and U10. The switches U11~U15 will be turned on. The relevant signals will be measured and verified to be within tolerance, and D1 through D5 will be visually verified. Resistive load will be applied to the Gantry Cabinet Power outputs at J42. Refer to the sheet 9 of UUT schematic.

8.8.1 Make sure +22.6Vdc is applied to J6-38 (MVDPUON#), J6-37 (KVDPUON#), J6-36 (KVSPUON#), J6-35 (BLADECONTON#)

8.8.2 Program the electronic load to draw 2.4 Amp of current

8.8.3 Close relay SW15 to apply electronic load to J42-2 (MDV24V)

8.8.4 +22.6Vdc will be removed from J6-38 (MVDPUON#),

8.8.5 Turn on the electronic load

8.8.6 The voltage at J42-2 (MDV24V) will be measured for 24Vdc ± 0.5Vdc

8.8.7 The voltage at J42-4 (KVD24V) will be measured for 0Vdc ± 0.5Vdc

8.8.8 The voltage at J42-6 (KVS24V) will be measured for 0Vdc ± 0.5Vdc

8.8.9 Verify that D5 is illuminated and D4, D3 are not illuminated

8.8.10 Turn off the electronic load

8.8.11 +22.6Vdc will be applied to J6-38 (MVDPUON#)

8.8.12 Open SW15 to disconnect the load.

8.8.13 Close relay SW16 to apply electronic load to J42-4 (KVD24V)

8.8.14 +22.6Vdc will be removed from J6-37 (KVDPUON#)

8.8.15 Turn on the electronic load

8.8.16 The voltage at J42-2 (MDV24V) will be measured for 0Vdc ± 0.5Vdc

8.8.17 The voltage at J42-4 (KVD24V) will be measured for 24Vdc ± 0.5Vdc

8.8.18 The voltage at J42-6 (KVS24V) will be measured for 0Vdc ± 0.5Vdc

8.8.19 Verify that D4 is illuminated and D5, D3 are not illuminated

8.8.20 Turn off the electronic load

8.8.21 +22.6Vdc will be applied to J6-37 (KVDPUON#)

8.8.22 Open SW16 to disconnect the load.

8.8.23 Close relay SW17 to apply electronic load to J42-6 (KVS24V)

8.8.24 +22.6Vdc will be removed from J6-36 (KVSPUON#)

8.8.25 Turn on the electronic load

8.8.26 The voltage at J42-6 (KVS24V) will be measured for 24Vdc ± 0.5Vdc

8.8.27 The voltage at J42-8 (BLADE) will be measured for 0Vdc ± 0.5Vdc

8.8.28 The voltage at J42-11 (BLADEPWR) will be measured for 0Vdc ± 0.5Vdc

8.8.29 Verify that D3 is illuminated and D2 is not illuminated

8.8.30 Turn off the electronic load

8.8.31 The signal at J8-14 (BLADEPWRSTS) will be measured for logic low

8.8.32 Verify that D1 is not illuminated

8.8.33 +22.6Vdc will be applied to J6-36 (KVSPUON#)

8.8.34 Open SW17 to disconnect the load.

8.8.35 Close relay SW18 to apply electronic load to J42-8 (BLADE)

8.8.36 +22.6Vdc will be removed from J6-35 (BLADECONTON#)

8.8.37 Turn on the electronic load

8.8.38 The voltage at J42-8 (BLADE) will be measured for 24Vdc ± 0.5Vdc

8.8.39 Verify that D2 is illuminated

8.8.40 Turn off the electronic load

8.8.41 Open SW18 to disconnect the load.

8.8.42 Close relay SW19 to apply 9.3 ohm resistive load to J42-11 (BLADEPWR)

8.8.43 The voltage at J42-11 (BLADEPWR) will be measured for 27Vdc to 30Vdc

8.8.44 The signal at J8-14 (BLADEPWRSTS) will be measured for logic high

8.8.45 Verify that D1 is illuminated

8.8.46 +22.6Vdc will be applied to J6-35 (BLADECONTON#)

8.8.47 Open SW19 to disconnect the load.

## Lamps Test

This test will verify the operation of the lamps circuit, which consists of U42, U17, U57, U58, U55 and U56. The field lamp will be turned on by the control signal. During the verification of the Field lamp soft start circuit, electronic load will be applied to J5\_3. This test also verifies the J49. Refer to the sheet 10 of the UUT schematic.

8.9.1 Program the electronic load to CR mode at 2 ohm.

8.9.2 Close relay SW20 to connect the electronic load to J5-1(FLAMP1)

8.9.3 +22.6Vdc will be applied to J6-19 (FLAMPSSON) and J6-18 (FLAMP1CTRL) to turn on U42 and U67

8.9.4 Turn on the electronic load

8.9.5 Use DMM to measure output voltage at FLAMP1

8.9.6 The voltage at J5-1 (FLAMP1) will be measured with system lamps and cables for 5.4 to 7.0VDC

8.9.7 The voltage at J5-3 (FLAMP2) will be measured with system lamps and cables for -0.10 to +0.75Vdc

8.9.8 Increase the programmed load conductance from electronic load by 0.05S steps, while monitor the output voltage at FLAMP1. This voltage shall remain stable for 5.5 to 7.0VDC

8.9.9 Keep increase the load conductance by 0.05S, until either the output dropped to below 5.5V or load conductance is above 1S (resistance < 1.0ohm). Verify that shut-down load current is below 5.2A.

8.9.10 Turn off the electronic load

8.9.11 Open the relay SW20 to disconnect electronic load from J5-1(FLAMP1)

8.9.12 The 22.6Vdc will be removed from J6-19 (FLAMPSSON) and J6-18 (FLAMP1CTRL) to turn off U42 and U57. Wait 10 Sec.

8.9.13 Program the electronic load to CR mode at conductance = 0.18S

8.9.14 Close relay SW21 to connect the electronic load to J5-3(FLAMP2)

8.9.15 +22.6Vdc will be applied to J6-19 (FLAMPSSON) and J6-40 (FLAMP2CTRL) to turn on U42 and U58

8.9.16 Turn on the electronic load

8.9.17 The voltage at J5-3 (FLAMP2) will be measured with system lamps and cables for 5.37 to 5.79VDC

8.9.18 The voltage at J5-1 (FLAMP1) will be measured with system lamps and cables for -0.10 to +0.75Vdc

8.9.19 The voltage at daughter card monitor point AI\_MF0 will be measured for 1.59125 to 1.75875V

8.9.20 The voltage at daughter card monitor point AI\_MF2 will be measured for 1.800 to 2.200V

8.9.21 Turn off the electronic load

8.9.22 Open the relay SW21 to disconnect electronic load from J5-3(FLAMP2)

8.9.23 The +22.6Vdc will be removed from J6-19 (FLAMPSSON) and J6-40 (FLAMP2CTRL) to turn off U42 and U58

8.9.24 Keep J49-1 and J49-2 open, check J49-1 for 24Vdc ± 0.5Vdc

8.9.25 The signal at J8-6 (GNT\_MONSWSTS) will be measured for logic low

8.9.26 Close the switch between J49-1 and J49-2

8.9.27 The signal at J8-6 (GNT\_MONSWSTS) will be measured for logic high

8.9.28 Open switch between J49-1 and J49-2

## EEPROM Test

This test will verify the operation of the serial EEPROM U1. The signals of the EEPROM are controlled by DSP on DPD\_PCB. During the test, three tests will be implemented, which are the address range test, the data array test and the zero test. Refer to the sheet 7 of the UUT schematic.

8.10.1 The address range test of the EEPROM will be performed by writing a unique data value to each EEPORM page. The EEPROM has 256-page; each page has 32-byte. In this test, the data value will be written started with 0 and increment by one for each new page. For instance, page 1 will be written with the value of 0, page 2 will be written with the value of 1, and last page 256 will be written with 256. The test will verify that all EEPROM addresses can be accessed by reading the data back from each address and calculating the sum of the reading data, and verify the sum of data is equal to 1,144,480.

8.10.2 0x55 will be written to the EEPROM data array. The data pattern will be read from each address location and verified for 0x55

8.10.3 0xAA will be written to the EEPROM data array. The data pattern will be read from each address location and verified for 0xAA

8.10.4 0x00 will be written to the EEPROM data array. The data pattern will be read from each address location and verified for 0x00

## Program Serial EEPROM

If the UUT passes all of the tests in the test groups above then the Serial EEPRON U1 will be programmed with the data structure outlined in document:100041411-02.

## Shutdown

8.12.1 All the AC and DC power sources will be turned off

8.12.2 Disconnect all fixture connector cables from the UUT

8.12.3 Remove the DPD\_PCB from the UUT

8.12.4 Remove the UUT from the test fixture

8.12.5 The functional test is complete